TSMC-02-1033

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January 13, 2004

To: Commissioner for Patents

P.O.Box 1450

Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572

28 Davis Avenue

Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/696,006 10/29/03

Kuo-Chi Tu

STRUCTURE FOR REDUCING LEAKAGE CURRENTS AND HIGH CONTACT RESISTANCE FOR EMBEDDED MEMORY AND METHOD FOR MAKING SAME

## INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

## CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

TSMC-02-1033

- U.S. Patent 6,403,417 to Chien et al., "Method for In-situ Fabrication of a Landing Via and a Strip Contact in an Embedded Memory," describes a method for making via holes and strip contact holes for embedded memory.
- U.S. Patent 6,485,988 to Ma et al., "Hydrogen-free Contact Etch for Ferroelectric Capacitor Formation," describes a method for using a hydrogen-free contact etch for ferroelectric capacitor formation.

Sincerely

Stephen B. Ackerman, Reg. No. 37761

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